REMARKS

Applicant has reviewed the Final Office Action dated April 17, 2008, and the references cited therein. Applicant has amended the claims to address informalities cited in the Office Action. **Claims 1-3 and 5-13** were previously pending and none were allowed. The claims have been amended to address the *Claim Objections* raised at page 2 of the Office Action. Claim 8 has been amended to address the Section 112, paragraph 2, rejection raised on page 3 of the Office Action. Moreover, Applicant has amended independent claims 1 and 8 to more clearly define the origin of the "second identifier" element.

In view of the amendments, Applicant submits that the presently pending claims are patentable over the presently known prior art. Accordingly, Applicant requests favorable reconsideration of the previous objections and rejections in view of Applicant's amendments.

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Summary of The Prior Art-Based Claim Rejections

The following identifies the authority and prior art applied to the identified claims for each rejection of the claims set forth in the Office Action.

1. Claims 1-3, 5-6 and 8-12 are rejected under 35 U.S.C. §102(b) as being unpatentable over Karp U.S. Pat. No. 5,748,936 (Karp), in view of Kogge, "The Microprogramming of Pipelined Processors," 1981.
2. Claim 7 and 13 are rejected under 35 U.S.C. §103(a) as being unpatentable over Karp in view of Kogge and further in view of the Examiner's taking of Official Notice.

Applicant traverses each of the grounds for the rejection of the presently pending claims for the reasons set forth herein below.

Reasons for Traversing the Current Rejections of the Claims

Applicant traverses the rejection of claims 1-3, 5-6 and 8-12 as being obvious over Karp in view of Kogge since the invention recited in the independent claims (1 and 8) is not rendered by the combined teachings of these references. Applicant respectfully submits that, indeed, the subject-matter of the present invention and the disclosure by Karp achieve substantially differing results.

The Cited Karp Reference

Karp, upon which the Final Office Action primarily relies, aims to improve the degree of instruction level parallelism at a VLIW processor by speculative execution of conditional operations. Karp discloses a system wherein during speculative execution of conditional operations, exceptions may occur that should be taken into account if the condition for the conditional operation turns out to be true. If the condition turns out to be false, the exception should be ignored. To that end Karp provides for a speculative look aside table (SLAT) 80 wherein a poison bit indicates whether an exception has occurred, and the SLAT is accessed via a predicate file 50.

Summary of the Presently Claimed Invention

In contrast to Karp's speculative execution, exception detection and poison bit arrangement, Applicant's claimed invention does not relate to speculative execution. Rather, as explained by Applicant in the Background of the invention, "The compiler combines instructions into a VLIW instruction under the constraint that the instructions assigned to a single VLIW instruction can be executed in parallel and under data dependency constraints." *See*, Applicant's Specification at page 2, lines 11-13.

The previous Office Action response submitted by Applicant's representative on February 11, 2008, stated that the processor may handle a conditional instruction MODULO(A,C). This operation is often used in address calculations. The calculation is carried out for values of $C > 0$ and for values of A in the range between -2C and 2C-1. The result R of the MODULO(A,C) operation can be defined in c-code as follows:

If $(A-C)>0$ then $R = A-C$

If $(A+C)<0$ then $R = A+C$

In the claimed time-stationary processor embodying the present invention, the MODULO operation described above can be implemented on a combination of a first execution unit and a second execution unit. The first execution unit calculates the function POSDIFF(A,C) as $R = A - C$ and provides an identifier on the validity of the relation $(A-C) > 0$. The second execution unit calculates the function NEGSUM(A,C) as $R = A + C$ and provides an identifier on the validity of the relation $(A+C) < 0$. Based on the value of A and C

either the outcome of the first functional unit, the outcome of the second functional unit, or none of these outcomes is written into the register file.

For the above-mentioned range of values of C > 0 the conditional results are mutually exclusive. Intrinsically, the conditions (A-C), (A+C) that respectively indicate the validity of the operations R=A-C and R=A+C are only available after completion of these operations.

Karp Does Not Disclose Applicant's Claimed "Second Identifier" (Rendered by a Programmable Criterion)

Applicant's claimed "second identifier" differs from the "exceptions" and "poison bit" described in Karp and referenced in the Office Action's rejection of independent **claims 1 and 8**. Karp's disclosed poison bit value merely indicates whether earlier in an instruction stream an exception was generated. See, Karp, Figure 5, blocks 212, 214. The poison bit, resulting from the generation of an exception, cannot be used for Applicant's claimed custom operation – in particular Applicant's recited "dynamically control writing of result data corresponding to an operation into the register file."

In a processor incorporating *Applicant's claimed invention*, a programmer dictates, via a *programmable criterion*, conditions under which a valid operation has occurred. In the processor disclosed in Karp, there is a fixed/predetermined (i.e., non-programmable) set of conditions, usually defined by the machine architecture, that result in an exception and thereafter a setting of the poison bit. This essential difference is clarified in claims 1 and 8 by specifying that the *second identifier* is produced *according to a programmable criterion.*

The Prior Art References Do Not Disclose Applicant's Claimed "First Identifier"

Furthermore, Applicant submits that the invention recited in dependent **claims 2 and 9** is not disclosed in the combined teachings of the cited prior art references. In the processor according to an embodiment of the present invention, an unnecessarily large code-size is avoided by indicating the absence of instructions, i.e. NOP operations, by single bits in a header attached to the front of the VLIW instruction. In the illustrative embodiment of the invention recited in claims 2 and 9, *a first identifier* is used to indicate the presence of a NOP and therewith to disable the writing back of result data. Moreover, the first identifier is delayed according to the pipeline arranged for executing the operation. By delaying the first identifier according to the pipeline of the execution unit, the information required for

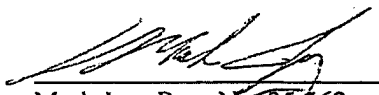
determining the write back of result data becomes available at the output of the execution unit at the same time as the result data itself. The latter result, incorporated into the recited elements of claims 2 and 9, is by no means disclosed by Karp. In fact Karp points away from this measure. Karp, at col. 10, lines 16-21, states that the predicate may not be known until later because it is being computed as the current operation proceeds through the pipeline process. On the contrary, in the processor according to the present invention the first identifier is known, but it is delayed.

Thus, in summary, the invention recited in presently pending independent claims 1 and 8 (and dependent claims 2 and 9) provides a novel and inventive way to enable *programmable* conditional dynamic write operations in a time-stationary processor. The claimed invention enables custom operations to be executed by the execution unit that potentially produce more than one valid output.

The rejections of each of the presently pending *dependent claims* have been overcome by Applicant's current amendments to the independent claims. Applicant reserves the right to address the basis for the rejection of the dependent claims, if needed, at a later time in response to any further rejection of independent claims 1 and 8.

Applicant respectfully submits that the patent application is in condition for allowance. If, in the opinion of the Examiner, a telephone conference would expedite the prosecution of the subject application, the Examiner is invited to call the undersigned attorney.

Respectfully submitted,



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Date: September 17, 2008